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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/956,986	09/21/2001	Michiharu Matsui	214258US2S	2952

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EXAMINER	
TRAN, THIEN F	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 05/09/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/956,986	Applicant(s) MATSUI ET AL.	
	Examiner Thien Tran	Art Unit 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 March 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-62* is/are pending in the application.

4a) Of the above claim(s) *2,4,6,8-10,12,13,15-31,33,35 and 37-60* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,5,7,11,14,32,34,36,61 and 62* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *03 March 2003* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *13* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 3, 5, 7, 32, 34, 36, 61 and 62 are rejected under 35 U.S.C. 102(e) as being anticipated by Shimizu et al. (USPN 6,342,715).

Shimizu et al. discloses the claimed semiconductor device (Figs. 60, 61A, 61B, 62A) comprising a semiconductor layer 1; a first insulating film 54 formed on said semiconductor layer; a first electrode layer 55 formed on said first insulating film; an element isolating region 2 comprising an element isolating insulating film formed to extend through said first electrode layer and said first insulating film to reach an inner region of said semiconductor layer, said element isolating region isolating an element region and being self-aligned with said first electrode layer; a second insulating film 6 formed on said first electrode layer and said element isolating region, an open portion exposing a surface of said first electrode layer being formed in said second insulating film; and a second electrode layer 57 formed on said second insulating film and said exposed surface of said first electrode layer, said second electrode layer being electrically connected to said first electrode layer via said open portion, said first and

second electrode layers including a gate electrode, said open portion having a first width in a direction of a gate length of said gate electrode and a second width in a direction perpendicular to the direction of the gate length, the second width being greater than the first width.

Regarding claim 3, said gate electrode is a gate electrode 58 of a selective transistor included in a NAND type flash memory.

Regarding claim 5, Shimizu et al. further discloses a semiconductor device (Fig. 62B) in a memory cell array region comprising said semiconductor layer 1; said first insulating film 42 formed on said semiconductor layer; said first electrode layer 5 formed on said first insulating film; said element isolating region 2 comprising an element isolating insulating film formed to extend through said first electrode layer and said first insulating film to reach an inner region of said semiconductor layer, said element isolating region isolating an element region and being self-aligned with said first electrode layer; said second insulating film 6 formed on said first electrode layer and said element isolating region; and said second electrode layer 7 formed on said second insulating film; wherein a surface of said element isolating region of said memory cell array region is arranged below a surface of said first electrode layer.

Regarding claim 7, said first electrode layer 5 performs a function of a floating gate and said second electrode layer 7 performs a function of a control gate in said memory cell array region.

Regarding claim 32, the first electrode layer 55 formed of polysilicon film 13 and the second electrode layer 57 formed of metal silicide film 19, which achieves lower resistance.

Regarding claim 34, said second insulating film 6 comprises of a complex insulating film including a silicon nitride film.

Regarding claim 36, said second insulating film 6 remains at an edge portion of said gate electrode.

Regarding claim 61, said open portion extends over element regions identical to said element region, in the direction perpendicular to the length of the gate length.

Regarding claim 62, said element isolating insulating film 2 is provided between said element regions, and includes a groove formed in said element isolating insulating film (Fig. 61A), and said groove is located under said open portion, and has a same shape as said open portion.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 11 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimizu et al. (USPN 6,342,715) in view of Admitted prior art (APA).

Shimizu et al. as described above does not disclose a connecting member arranged above said element isolating region 2 and a wiring electrically connected to

said second electrode layer 57 via said connecting member so that a voltage can be applied to the gate electrode. It is old and well known to form an interconnect comprising a wiring and a connecting member arranged above an element isolation region as shown for example by APA (Fig. 49B). APA discloses a connecting member 20 arranged above an element isolating region 15 and electrically connected to a second electrode layer 18, and a wiring 21 electrically connected to said second electrode layer 18 via the connecting member 20, wherein said wiring and a first electrode layer 13 are connected to each other via said second electrode layer 18 extending from said element region onto said element isolating region. It would have been obvious to a person having ordinary skill in the art to form a wiring and a connecting member as taught by APA above the element isolating region 2 of Shimizu et al. so that the first electrode layer 55 can be electrically connected to an external source (voltage) through the second electrode layer 57, the connecting member and the wiring in order for the selective transistor to be operated.

Response to Arguments

Applicant's arguments with respect to claims 1, 3, 5, 7, 11, 14, 32, 34, 36, 61 and 62 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thien Tran whose telephone number is (703) 308-4108. The examiner can normally be reached on 8:30AM - 5:00PM Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

tt
May 6, 2003

Thien Tran
Patent Examiner
Technology Center 2800